A DYNAMICALLY PROGRAMMABLE INTEGRATED SWITCHING DEVICE USING AN ASYMMETRIC 5T1C CELL

ABSTRACT:

[0051] A switching element including first, second and third ports each comprising a plurality of lines is disclosed. A first memory cell includes a storage element, a first pass gate for selectively coupling a first line of the first port to the storage element, a second pass gate for selectively coupling a first line of the second port to the storage element, and a third pass gate for selectively coupling a first line of the third port to the storage element. A second memory cell includes a storage element, a first gate for selectively coupling a second line of the first port to the storage element, a second pass gate for selectively coupling a second line of the second port to the storage element, and a third pass gate for selectively coupling a second line of the third port to the storage element.